ZIHAO, CHEN

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EDUCATION

Fudan University **Shanghai, China**

M.S & Ph.D. student *in Electronic Science and Technology* Sep. 2021 – Jun. 2026 (Expected)

- GPA: 3.70/4.0 (top 5%); mentored by Prof. Fan Yang (directly) and Prof. Xuan Zeng
- Research interests: AI techniques like large language models (LLMs) & reinforcement learning (RL), and their applications in electronic design automation (EDA)

B.E. *in Microelectronic Science and Engineering* Sep. 2017 – Jun. 2021

- GPA: 3.72/4.0 (top 5%)

SELECTED PUBLICATIONS

Zihao Chen, Zihan Lin, Xinhua Chen, Zhiyi Liu, Changxu Liu, Yuxuan Qiao, Yifei Feng, Junjie Zuo, Yifan Song, and Fan Yang, "Spec2Doc2RTL: RTL Generation from Specification with Natural Language Representation," *International Symposium of Electronic Design Automation (ISEDA)*, 2025.

Zihao Chen, Jiangli Huang, Yiting Liu, Fan Yang, Li Shang, Dian Zhou, and Xuan Zeng, "Artisan: Automated Operational Amplifier Design via Domain-specific Large Language Model," *Design Automation Conference (DAC)*, 2024.

Zihao Chen, Songlei Meng, Fan Yang, Li Shang, and Xuan Zeng, "MACRO: Multi-agent Reinforcement Learning-based Cross-layer Optimization of Operational Amplifier," *Asia and South Pacific Design Automation Conference (ASPDAC)*, 2024.

Zihao Chen, Songlei Meng, Fan Yang, Li Shang, and Xuan Zeng, "TOTAL: Topology Optimization of Operational Amplifier via Reinforcement Learning," *International Symposium on Quality Electronic Design (ISQED)*, 2023.

Zihao Chen, Fan Yang, Li Shang, and Xuan Zeng, "Automated and Agile Design of Layout Hotspot Detector via Neural Architecture Search," *Design, Automation and Test in Europe (DATE)*, 2023.

Jinyi Shen, **Zihao Chen**, Ji Zhuang, Jiangli Huang, Fan Yang, Li Shang, Zhaori Bi, Changhao Yan, Dian Zhou, Xuan Zeng, "Atelier: An Automated Analog Circuit Design Framework via Multiple Large Language Model-based Agents," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, under review, 2025.

Zhengqi Gao, **Zihao Chen**, Jun Tao, Yangfeng Sun, Dian Zhou, and Xuan Zeng, "Bayesian Inference on Introduced General Region: An Efficient Parametric Yield Estimation Method for Integrated Circuits," *Asia and South Pacific Design Automation Conference (ASPDAC)*, 2021.

Zheng Wu, Zhuochu Yang, Zhuoyuan Yang, **Zihao Chen**, Li Shang, and Fan Yang, "ChatArch: A Knowledge-based Graph-of-thought LLM Framework for Processor Architecture Design," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, under review, 2025.

MAIN RESEARCH EXPERIENCE

Fudan University (State Key Laboratory of Integrated Chips and Systems) **Shanghai, China**

Research Assistant to Prof. Fan Yang Feb. 2021 – Jun. 2026 (Expected)

- **A Light-weight Fundamental LLM for Analog Circuit Design**

We are training the first fundamental LLM for analog circuit design. To address the scarcity of analog circuit data, we collect a substantial amount of high-quality literature, covering various learning stages and circuit types. In response to the complexity of data modalities, we construct a multi-agent framework that normalizes image information into text with manual checking. Given the complexity of analog circuit knowledge, we structure the data into a knowledge graph and systematically generated comprehensive fine-tuning data and benchmarks. Experimental results shows that the model, derived from continual pre-training (CPT) and supervised fine-tuning (SFT) on llama3-8b, shows competitive accuracy on the benchmark. ***This project is ongoing.***

- **An LLM-based RTL Testbench Generation Framework with Reasoning Techniques**

In the exploration of using LLMs for digital circuit design, the automatic generation of testbenches for new circuits presents a challenge. Early efforts only established basic testbench generation and debugging workflows, lacking sufficient integration of domain knowledge and full utilization of the reasoning capabilities of LLMs. We construct a reliable chain of thought (CoT) for agents based on domain knowledge, driving the LLM to generate testbenches step by step. Now we are trying to employ heuristic algorithms such as tree search for test-time scaling (TTS) to enhance the reasoning and error-correction of the LLM, thereby generating high-quality testbenches. ***This project is ongoing.***

- **Spec2Doc2RTL: An LLM-based RTL Generation Framework Using Natural Language Representation**

Recent RTL code generation efforts focus on constructing SFT datasets to directly generate RTL code from design specifications (Spec). We propose Spec2Doc2RTL, employing natural language, rather than RTL code, as the design representation. This approach decomposes the RTL code generation task into two steps that LLMs are more adept at: design document completion (Spec2Doc) and RTL code translation (Doc2RTL). We implement a hierarchical recursive design process with testbench generation mechanism to achieve end-to-end RTL generation. Experimental results show that the framework based on GPT-4o, can not only design system-level circuits such as NTT and CPU, but also surpasses the baselines for small module design. ***This work will be published at ISEDA'25.***

- **Artisan: An Automated Operational Amplifier Design Framework with Domain-Specific LLMs**

We propose Artisan, taking operational amplifier (opamp) as an example, to apply LLMs to analog circuit design for the first time. We introduce a bidirectional representation technique that aligns circuit netlists with corresponding structural and functional descriptions, enabling LLMs to understand circuits. Then we model the design process into a CoT based on domain knowledge and construct it as a multi-turn dialogue dataset, driving the LLM to learn through SFT. Experimental results show that the model trained on llama2-7b significantly surpasses existing methods. ***This work is published at DAC'24.***

- **TOTAL & MACRO: Reinforcement Learning-based Operational Amplifier Design**

We propose TOTAL, an RL-based method for opamp topology generation. To address the high-dimensionality of the design space, we decompose the opamp design into a Markov decision process where the agent incrementally modifies the topology. To tackle the discreteness of the design space, we construct the agent with a GNN-CNN structure to represent the current design state (GNN) and predict the next action (CNN). To solve the reward sparsity, we design a scoring function to guide the agent evolving in the correct direction. Experimental results show that TOTAL surpasses all baselines. ***This work is published at ISQED'23.***

Subsequently, we propose MACRO, a multi-agent RL framework for topology-parameter co-optimization of opamps. Building on TOTAL, the problem of optimizing parameters for a given topology is assigned to another agent, and these two agents are trained collaboratively. Experimental results show that MACRO outperforms TOTAL. ***This work is published at ASPDAC'24.***

- **A Layout Hotspot Detector Agile Design Method with Neural Architecture Search in the Latent Space**

We propose an agile generation method for hotspot detectors based on Neural Architecture Search (NAS). Specifically, we pre-train a variational autoencoder (VAE) and a performance predictor to transform the discrete NN topology design space into a continuous latent space. Gradient methods are then employed to find the optimal solution in the latent space, which is then decoded into the NN topology. Experimental results show that this method significantly improves design speed while achieving competitive performance. ***The work is published at DATE'23.***

TEACHING SERVICES

Fudan University **Shanghai, China**

- TA for *LLMs and Their Applications in Electronic System Design Automation* (instructor: Prof. Fan Yang) 2025
- TA for *Fundamentals of Digital Integrated Circuit Design Automation* (instructor: Prof. Fan Yang) 2022, 2023, 2024, 2025
- TA for *Programming Basics* (instructor: Prof. Fan Yang) 2021, 2022, 2023, 2024
- TA for *Fundamentals of Computer Software* (instructor: Prof. Xuan Zeng) 2022

OTHER SERVICES

- **Reviewer**, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)* 2025
- **Reviewer**, *ACM Transactions on Design Automation of Electronic Systems (TODAES)* 2024, 2025
- **Organizer**, 1st LLM4EDA Summer School, State Key Lab. of Integrated Chips & Systems, Fudan University 2024

SELECTED HONORS

- Outstanding Student, Fudan University 2019, 2020, 2021, 2022, 2024
- KLA scholarship (top 1%), Fudan University 2023
- Outstanding TA, Fudan University 2023
- First prize scholarship (top 5%), Fudan University 2019

SKILLS

- Programming: Python (specifically Pytorch), C/C++, MATLAB
- Hardware: HSPICE, VerilogA
- Languages: Mandarin Chinese (native), English (proficient in both writing and oral communication)